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A Compact 5 GHz Lumped-Element Wilkinson Power Combiner on 28 nm Bulk CMOS

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Abstract—A novel lumped-element Wilkinson power combiner designed at 5 GHz on a 28 nm bulk CMOS process is presented. The core circuit requires only three components with two additional capacitors used to implement a second harmonic trap, further reducing the circuit area and output distortion. The circuit uses a single coupled coil to provide two series inductances used in the combiner. Additionally, the coil parasitics provide the isolation resistance, removing the need for a discrete resistor. Design equations and methodology for the coupled coil are given along with integrated circuit (IC) measurement results. Return losses (RL) and isolation are greater than 10.1 dB from 4.3 GHz to 5.3 GHz with the insertion loss (IL) lower than 1.2 dB. The active circuit dimensions are $261 \mu\text{m} \times 346 \mu\text{m}$ giving an area of 0.09 mm^2 .

Index Terms—28 nm, 5 GHz, CMOS, lumped element, Wilkinson power combiner

I. INTRODUCTION

The output power capability of CMOS power amplifiers (PA) is limited by the low drain breakdown voltages of CMOS transistors which in turn imposes the use of low supply voltages. This issue can be addressed by employing a larger transistor that can draw additional current, thus compensating for the low supply voltage. However, large transistors are prone to instability and are very sensitive to process variations. Furthermore, large transistors have very low drain impedances which increases the matching losses. Additionally, thermal management issues arise with the use of a single large transistor due to the large amount of current flowing through a small area.

An elegant solution to these problems consists of using multiple CMOS PA unit cells whose output power is combined using power combiners such as the Wilkinson power combiner (WPC) thus increasing the output power capability of CMOS PAs and lessening the heat-sinking requirements as the use of multiple PA unit cells enables an even distribution of heat across the circuit area. However, in the classical WPC, shown in Fig. 1a, the quarter-wave transmission lines are excessively large when fabricated on a CMOS process, e.g. 7.6 mm at 5 GHz, and thus are unsuitable for IC implementation. To address this problem, a lumped-element WPC, as shown in Fig. 1b, can be used. The implementation of the proposed

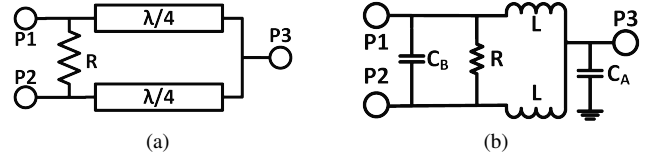


Fig. 1. WPC schematics (a) Distributed (b) Lumped

lumped-element WPC on a CMOS process requires the use of spiral inductors which occupy a large circuit area and have high losses due to the thin metal layers available on CMOS processes and the low resistivity CMOS substrate. To reduce the required inductor area, mutual coupling has been used in [1]–[4] to increase the inductance density. However, the effect of coupling parasitics, which degrades the RLs and the isolation of the WPC, was not taken into account.

In this paper, mutual coupling is used in the design of a novel WPC while taking into account the effect of the coupling parasitics. Additionally, the isolation resistance is entirely provided by the coil parasitics and can be tuned to desired values. This results in a WPC design requiring only three components which is, to the authors' knowledge, a record low in component count for a lumped-element WPC. Furthermore, a second harmonic trap can be integrated to reduce the output signal distortion and the physical size, and this design is the focus of the paper. The proposed WPC was implemented on an advanced 28 nm bulk CMOS process with a $2.8 \mu\text{m}$ thick aluminium top metal layer.

II. COUPLED COIL THEORY

To provide the two inductances in Fig. 1b, a three-port coil can be used with two sets of windings connected to a common input. Three-port coupled coils can be modelled as star or delta networks which are equivalent to two-port T and π networks respectively. The coupled coils can either undergo non-inverting or inverting coupling which is caused by adjacent currents flowing in the same or opposite direction respectively. Models of three-port coupled coils are shown in Fig. 2 where L_x is the self-inductance of each branch and M is the mutual inductance between the two branches which is defined in terms of the coupling factor k in (1). To derive the models in Fig. 2, the star networks use the conventional two-port T network model of a coupled coil while the delta networks were derived using a star-delta transformation.

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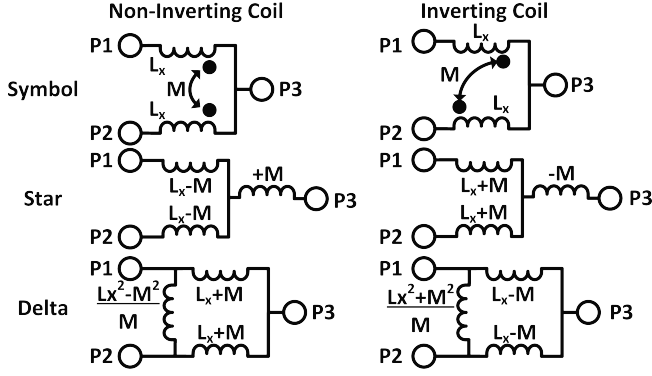


Fig. 2. Non-inverting and inverting coil models

$$M = kL_x \quad (1)$$

It can be seen in Fig. 2 that the two inductive branches of the star inverting coil and the delta non-inverting coils have larger net inductances when compared with their self-inductances. This increased inductance makes these two networks suitable for designing a compact lumped-element WPC as a smaller area is consumed to implement the required inductances. In addition to changing the overall coil inductance, the mutual coupling results in additional parasitic reactances which must be compensated for, otherwise the matching and isolation of the WPC will be severely compromised if implemented with a coupled coil. For the star inverting coil in Fig. 2, the negative inductance $-M$ connected to port 3 can be compensated with an additional series inductor M . The delta non-inverting coil in Fig. 2 has a parasitic inductance connected between ports 1 and 2 which can be resonated out at the fundamental frequency with a capacitor, defined in (2).

$$C_{\text{resonator}} = \frac{1}{\omega_0^2 \frac{L_x^2 - M^2}{M}} \quad (2)$$

To minimize the required area for the WPC in Fig. 1b, the delta non-inverting coil is the most suitable coil from Fig. 2 as the compensating capacitor requires a much smaller area and will have lower losses than the compensating inductor used in the star inverting coil.

III. NOVEL WPCS USING DELTA COUPLED COIL

The design equations for the WPC in Fig. 1b, obtained using even and odd mode analysis, are given in (3) with all ports matched to Z_0 .

$$(R, C_A, C_B, L) = \left(2Z_0, \frac{1}{\omega_0 Z_0}, \frac{1}{2\omega_0 Z_0}, \frac{Z_0}{\omega_0} \right) \quad (3)$$

To reduce the circuit area of the WPC in Fig. 1b, the two L inductors are replaced with a single delta non-inverting coil as in Fig. 3a. For the WPC circuit in Fig. 3a, $L_1 = L = L_x + M$, $C_1 = C_A$, and C_2 is defined as the combination of C_B from (3) and the resonating shunt capacitance from (2) which is required to remove the delta non-inverting coil's shunt parasitic

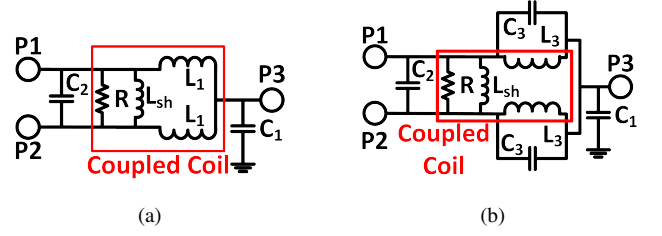


Fig. 3. WPC schematics (a) core (b) With second harmonic trap

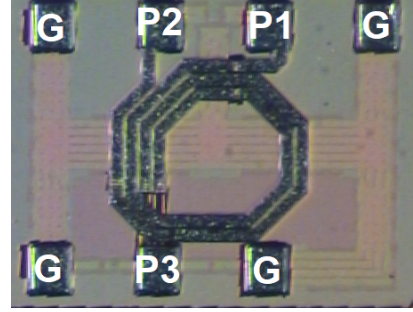


Fig. 4. Circuit micrograph

inductance ($L_{sh} = \frac{L_x^2 - M^2}{M}$). This capacitance C_2 is defined in (4).

$$C_2 = C_B + C_{\text{resonator}} \quad (4)$$

A key point to note when implementing the circuit in Fig. 3a is that the equivalent series resistance (ESR) of the shunt parasitic inductance increases as the coupling factor k is reduced. By tuning k , this resistance can provide R in (3), thus removing the need for a discrete resistor and simplifying the physical design of the circuit.

The design in Fig. 3a can have a second harmonic trap integrated by adding a capacitor in parallel with each inductive branch. The addition of a second harmonic trap reduces the distortion of the output signal and decreases the required inductance in each branch by 25% which will further reduce the size of the circuit. Fig. 3b shows a WPC based on Fig. 3a with a second harmonic trap added by replacing L_1 in Fig. 3a with the parallel LC network $L_3 C_3$, defined in (5), which is tuned to the second harmonic. At the fundamental frequency, $L_3 C_3$ is inductive and presents the required L from (3) to ensure correct matching between the input and output ports.

$$(L_3, C_3) = \left(\frac{3L}{4}, \frac{1}{4\omega_0^2 L_3} \right) \quad (5)$$

IV. 28 NM CMOS IMPLEMENTATION

The circuit in Fig. 3b was implemented in TSMC's 28 nm CMOS HPC process with a 2.8 μm top aluminium layer as shown in Fig. 4. The circuit (excluding the capacitors) was electromagnetically (EM) simulated in Keysight's Momentum with the capacitors simulated using the TSMC models. The circuit was designed to operate at 5 GHz with $Z_0 = 50 \Omega$, $L_3 = 1.46 \text{ nH}$, $C_1 = 0.44 \text{ pF}$, and $C_2 = 1.56 \text{ pF}$. The two resonating capacitors were independently tuned to maximise

the performance which resulted in $C_{3,P1} = 0.46$ pF and $C_{3,P2} = 0.34$ pF. As the coil is an edge-coupled design, the resistance R in (3) was fulfilled by tuning the spacing between the traces to tune k . The active circuit dimensions in Fig. 4 are $261 \mu\text{m} \times 346 \mu\text{m}$ giving an area of 0.09 mm^2 . C_1 was divided into two components for symmetry in the layout.

The S-parameter measurements were obtained using an Agilent E8361C PNA. Using a SOLT calibration, a Picoprobe Model 40A GSSG probe was connected to ports 1 and 2, and a Picoprobe Model 40A GSG probe was connected to port 3. The results, with the bond pads de-embedded using EM simulated S-parameters, are given in Figs. 5–11 and are summarised in Table I. There is excellent agreement between the simulations and measurements.

The circuit bandwidth is defined from 4.3 GHz to 5.3 GHz giving a fractional bandwidth of 21%. The input reflection coefficients, S_{11} and S_{22} , are lower than -10.5 dB and -12 dB across the bandwidth respectively with minima of -14 dB and -19.7 dB at 5.2 GHz and 5.1 GHz respectively. The output reflection coefficient, S_{33} , is excellent with a maximum value of -14.6 dB across the bandwidth with a minima of -18.9 dB at 5.3 GHz. The isolation, achieved without the use of a discrete resistor, is greater than 10.1 dB across the bandwidth and has a maxima of 16.7 dB at 5 GHz. Finally, the IL is lower than 1.2 dB across the bandwidth with a minima of 1 dB at 5 GHz. The second harmonic suppression level is -23 dB at 10.4 GHz, shifted slightly from 10 GHz in the simulations.

To the authors' knowledge, there have been no published lumped-element WPCs on an advanced 28 nm bulk CMOS process therefore no direct comparisons can be made. Table I compares the new WPC with some existing designs in the literature and it can be seen that the new design achieves excellent performance. The area of the WPC is very competitive, especially when considering the lower frequency of operation. Additionally, unlike in [1] and [5], the inputs of the new WPC are aligned on the same side making it much easier for the PAs to connect to it. The large second harmonic suppression is a key advantage of this design over [1] and [5].

V. CONCLUSION

A novel lumped-element Wilkinson power combiner using a coupled coil has been presented with design equations, methodology, and measurement results on TSMC's 28 nm bulk CMOS process. The design uses a novel three-port coupled coil to reduce the size of the circuit and the coil parasitics provide the isolation resistance without the need for a discrete resistor. The circuit achieves excellent performance as summarised in Table I.

REFERENCES

- [1] M. Caruso, A. Bevilacqua, and A. Neviani, "An X-band lumped-element Wilkinson combiner with embedded impedance transformation," *IEEE Microw. Wireless Compon. Lett.*, vol. 24, no. 10, pp. 689–691, Oct. 2014.
- [2] M. Balducci and H. Schumacher, "Ka band passive differential 4:1 power divider/combiner based on wilkinson topology," in *2017 13th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME)*, Jun. 2017, pp. 189–192.

TABLE I
COMPARISON WITH STATE-OF-THE-ART WPCs

	[1]	[5]	This work
Technology	350 nm	130 nm	28 nm
	SiGe	CMOS	CMOS
Frequency (GHz)	8 – 14	22 – 26	4.3 – 5.3
Bandwidth (%)	54	17	21
Input RL (dB)	> 10	> 13.8	> 10.5
Output RL (dB)	> 12	> 8.9	> 14.6
Isolation (dB)	> 10	> 14.8	> 10.1
IL (dB)	< 1.4	< 1.4	< 1.2
2 nd harmonic suppression (dB)	6.5	N/A	23
	(at 20 GHz)		(at 10.4 GHz)
Active area (mm ²)	0.12	0.035	0.09
$Z_{in}, Z_{out}(\Omega)$	60, 100	50, 50	50, 50

- [3] J. S. Park and H. Wang, "A fully differential ultra-compact broadband transformer-based Wilkinson power divider," *IEEE Microw. Wireless Compon. Lett.*, vol. 26, no. 4, pp. 255–257, Apr. 2016.
- [4] F. Wang and H. Wang, "An N-way transformer based Wilkinson power divider in CMOS," in *2016 IEEE MTT-S International Microwave Symposium (IMS)*, May 2016, pp. 1–4.
- [5] J. G. Kim and G. M. Rebeiz, "Miniature four-way and two-way 24 GHz Wilkinson power dividers in 0.13 μm CMOS," *IEEE Microw. Wireless Compon. Lett.*, vol. 17, no. 9, pp. 658–660, Sep. 2007.

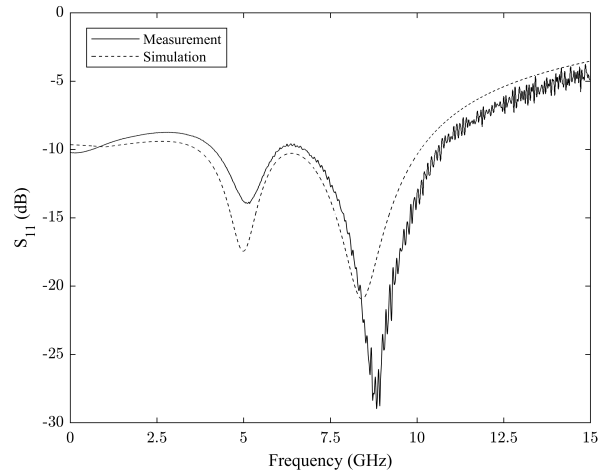


Fig. 5. Simulated and measured S_{11}

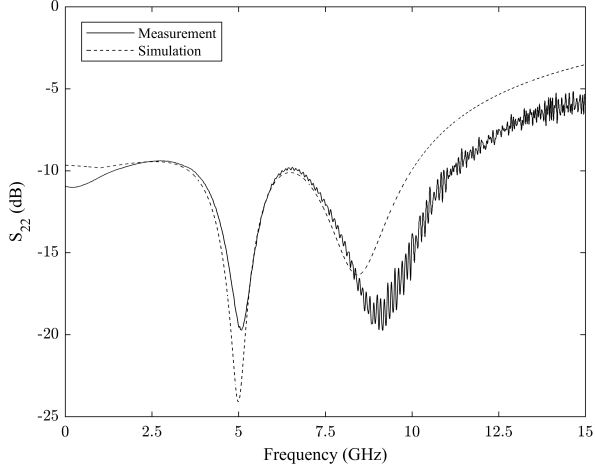
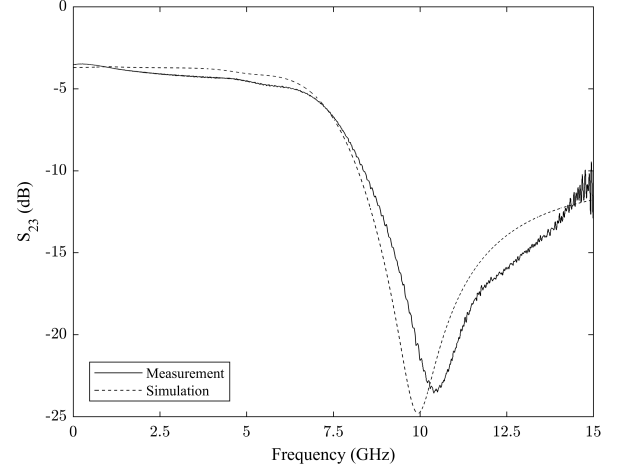
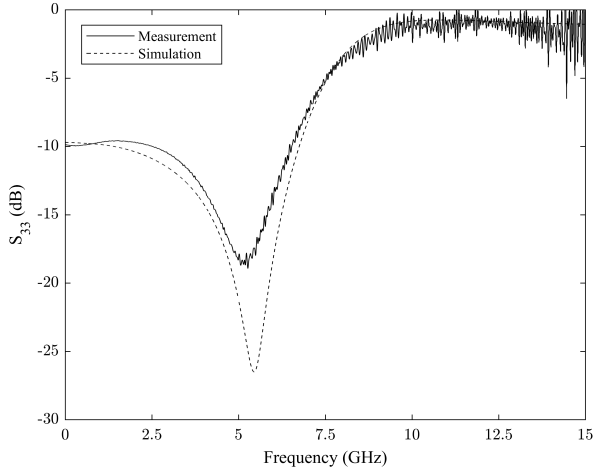
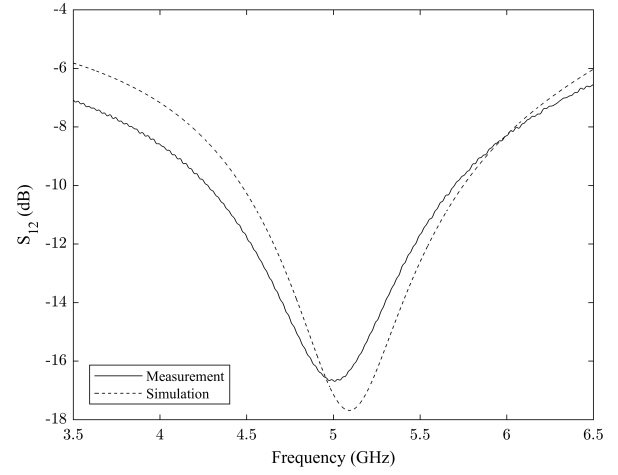
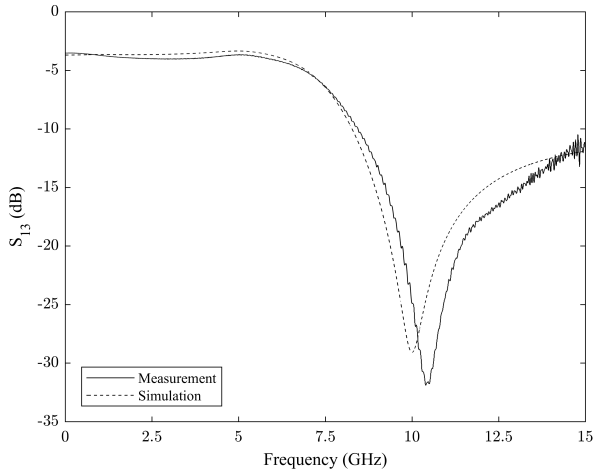
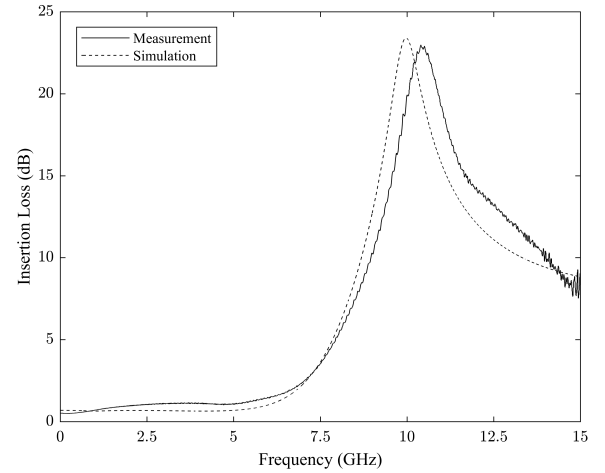
Fig. 6. Simulated and measured S_{22} Fig. 9. Simulated and measured S_{23} Fig. 7. Simulated and measured S_{33} Fig. 10. Simulated and measured S_{12} Fig. 8. Simulated and measured S_{13} 

Fig. 11. Simulated and measured insertion loss